REMARKS/ARGUMENTS

Claims 1-22 are pending in the present application. Claims 1, 3-5, 7-10, 12-17 and 19-22 have been amended to further clarify the invention. No claims have been added or canceled. Support for the amendments can be found, for example, from page 23, line 26 to page 24, line 15. Applicants have carefully considered the cited art and the Examiner's comments, and believe the claims patentably distinguish over the cited art and are allowable in their present form. Reconsideration of the rejection is, accordingly, respectfully requested in view of the above amendments and the following comments.

I. Information Disclosure Statement

The Examiner indicates that the three non-patent literature publications listed on the Information Disclosure Statement filed April 25, 2006, were not included with the IDS. We are herewith attaching copies of the missing articles, although a return postcard, a copy of which is enclosed, was received by Applicants indicating the references were received. A Supplemental Information Disclosure is also being filed concurrently. The Examiner is thanked for bringing this matter to Applicants' attention.

II. 35 U.S.C. § 102, Anticipation

The Examiner has rejected claims 1-6, 8-12, and 16-21 under 35 U.S.C. § 102(b) as being anticipated by Levine et al. (U.S. Patent No. 5,691,920). This rejection is respectfully traversed.

As to claim 1, the Examiner states:

> Referring to claim 1: Levine discloses a performance-monitoring unit (Abstract) and one or more hardware counters (column 10, lines 58-59) located within the performance monitoring unit (figure 4, structures 50 and 51). Levine discloses a variety of operations of the performance-monitoring unit (column 10, lines 34-56); Levine discloses setting the performance-monitoring unit to selectively monitor the instructions within specific addresses (column 12, 2nd paragraph). The instructions within specific addresses are a selected interrupt handling routine, and the Levine's selective monitoring on the particular instructions is the claimed hardware counters' counting the occurrence of events during an interrupt of a selected type. Furthermore, Levine discloses two separate counters for selected events (figure 6A, column 8, lines 57-60). Hence, the claim is anticipated by Levine.

Office Action dated May 18, 2006, pages 2-3.

Claim 1 of the present application as amended herein is as follows:

1. A data processing system for qualifying events when an interrupt occurs, comprising:
a performance monitoring unit;
one or more hardware counters located within the performance monitoring unit;

wherein the one or more hardware counters count the occurrence of events during processing of an interrupt of a selected type.

A prior art reference anticipates a claimed invention under 35 U.S.C. § 102 only if every element of the claimed invention is identically shown in that single prior art reference, arranged as they are in the claims. *In re Bond*, 910 F.2d 831, 832, 15 U.S.P.Q.2d 1566, 1567 (Fed. Cir. 1990). All limitations of a claimed invention must be considered when determining patentability. *In re Lowry*, 32 F.3d 1579, 1582, 32 U.S.P.Q.2d 1031, 1034 (Fed. Cir. 1994). Anticipation focuses on whether a claim reads on the product or process a prior art reference discloses, not on what the reference broadly teaches. *Kalman v. Kimberly-Clark Corp.*, 713 F.2d 760, 218 U.S.P.Q. 781 (Fed. Cir. 1983).

Applicants respectfully submit that Levine does not identically show every element of the claimed invention arranged as they are in the claims; and, accordingly, does not anticipate the claims. With respect to claim 1, in particular, Levine does not teach or suggest "one or more hardware counters located within the performance monitoring unit; wherein the one or more hardware counters count the occurrence of events during processing of an interrupt of a selected type".

Levine is directed to a method and system for "monitoring dispatch unit efficiency in a processing system" (column 1, lines 43-45). As noted by the Examiner, Levine lists a number of performance monitoring activities that may be performed in column 10, lines 34-39. None of the listed activities relate to counting events occurring during processing of an interrupt, and certainly none of the listed activities relate to counting the occurrence of events during processing of an interrupt of a selected type as recited in claim 1. Although, as pointed out by the Examiner, one of the listed performance monitoring activities in Levine is "identifying inhibited interrupts", monitoring inhibited interrupts, i.e., monitoring when interrupts are prevented or restrained, is not the same as counting "the occurrence of events during processing of an interrupt of a selected type". Levine does not count occurrences of events during processing of an interrupt of a selected type and contains no disclosure or suggestion of doing so.

Levine, in fact, appears to actually teach away from the Examiner's interpretation of the reference. In particular, in col. 3, lines 4-9, Levine states:

> Further, since the data gathered in accordance with the present invention occurs during real-time system processing, system designers have improved ability to more accurately determine specific deficiencies in system performance and develop system improvements to overcome these deficiencies.

This statement appears to confirm that Levine is designed to monitor activities during execution of a program and not during processing of an interrupt.

The Examiner refers to column 12, 2nd paragraph of Levine as disclosing "one or more hardware counters located within the performance monitoring unit; wherein the one or more hardware counters count the occurrence of events during an interrupt of a selected type". Applicants respectfully disagree. The second and third full paragraphs in column 12 of Levine are as follows:

> Bit 29 of MMCR1 is preferably used as a freeze counting until an IABR match signal occurs (FCUIABR) bit. An instruction address breakpoint register (IABR) match occurs while the IABR breakpoint is not enabled. For purposes of this discussion, the IABR refers to a register defined to hold an effective address that is used to compare with either a logical address of the instruction in the decode stage or the effective address of a branch target. In a preferred embodiment, the IABR is a supervisor-level register.
>
> Using bit 29 of MMCR1, a low logic level preferably indicates that counting is enabled. A high logic level in bit 29 preferably indicates that counting is disabled until an enabled IABR match occurs. To indicate that an IABR match is enabled, bits 0-4 of MMCR0 (counting enable bits) and the PM bit of the machine state register (MSR) are preferably used. Once the enabled IABR match occurs, bit 29 of MMCR1 is reset and counting occurs.

Nowhere does the above recitation disclose or suggest that any counter or counters in Levine counts "the occurrence of events during processing of an interrupt of a selected type". The Examiner alleges that the above recitation teaches that the "instructions within specific addresses are a selected interrupt handling routine", and, further, that "Levine's selective monitoring on the particular instructions is the claimed hardware counters' counting the occurrence of events during an interrupt of a selected type". Applicants' respectfully disagree.

The above recitation in Levine describes use of a bit 29 to enable and disable a counting operation. Nowhere in the cited paragraph of Levine, or anywhere else in Levine is there any teaching of "one or more hardware counters located within the performance monitoring unit; wherein the one or more hardware counters count the occurrence of events during processing of an interrupt of a selected type". Levine, therefore, does not disclose all claimed features of claim 1 and does not anticipate claim 1. Claim 1, accordingly, patentably distinguishes over Levine in its present form.

Claims 2-6 depend from and further restrict claim 1, and are also not anticipated by Levine, at least by virtue of their dependency. Furthermore, many of these claims recite additional subject matter that is not disclosed by Levine.

For example, as described above, Levine does not disclose "hardware counters that count the occurrence of events during an interrupt of a selected type"; and therefore also does not count the occurrence of events "during a state of the interrupt of the selected type" as recited in claim 2. Also, Levine does not disclose counting multiple types of events during the processing of the interrupt as recited in claim 4. Column 1, line 65 of Levine, referred to by the Examiner, only discusses monitoring a

processor's "instruction execution and storage control". This statement does not teach or enable "counting multiple types of events during the processing of the interrupt" as recited in claim 4. At least claims 2 and 4, accordingly, are allowable over Levine in their own right as well as by virtue of their dependency.

Independent claim 8 is as follows:

> 8. A method of executing instructions on an information processing system, comprising the steps of:
> receiving a signal at a microprocessor of the system for invoking an interrupt, wherein the interrupt includes a plurality of states; and
> counting at least one event for a selected state of the plurality of states during processing of the interrupt.

For similar reasons as discussed above with respect to claim 1, Levine does not disclose an interrupt that includes a plurality of states, and also does not disclose "counting at least one event for a selected state of the plurality of states during processing of the interrupt". Column 14, lines 63-65 of Levine referred to by the Examiner, recites:

> In order to effectively evaluate the flow of instructions through the processor's pipeline, all stages are preferably examined simultaneously.

This recitation is not a teaching of counting events for a selected state of a plurality of states during processing of an interrupt as required by claim 8. Claim 8, accordingly, is also not anticipated by Levine and is allowable over Levine in its present form; and it is respectfully requested that the Examiner so find.

Independent claim 16 recites similar subject matter as claim 8, and is also not anticipated by Levine for similar reasons as discussed above with respect to claim 8. Claims 9-12 and 17-21 depend from and further restrict one of claims 8 and 16 and are also not anticipated by Levine.

Therefore, the rejection of claims 1-6, 8-12 and 16-21 under 35 U.S.C. § 102 has been overcome.

III. 35 U.S.C. § 103, Obviousness – Claims 1-6, 8-14, and 16-21

The Examiner has rejected claims 1-6, 8-14, and 16-21 under 35 U.S.C. § 103(a) as being unpatentable over the admitted prior art in view of Levine et al. (U.S. Patent No. 5,691,920). This rejection is respectfully traversed.

In rejecting the claims, the Examiner states that the admitted prior art discloses a performance-monitoring unit and one or more hardware counters located within the performance-monitoring unit. The Examiner acknowledges that the admitted prior art doers not disclose that the one or more hardware counters count the occurrence of events during an interrupt of a selected type. The Examiner asserts, however:

> Levine discloses a variety of operations of the performance-monitoring unit (column 10, lines 34-39); Levine discloses setting the performance-monitoring unit to selectively monitor the instructions within specific addresses (column 12, 2nd paragraph). The instructions within specific addresses are a selected interrupt handling routine, and the Levine's selective monitoring on the particular instructions is the claimed hardware counters' counting the occurrence of events during an interrupt of a selected type. Levine teaches one to analyze the system performance and to focus particular sets of instructions for examining the performance bottleneck. Hence, it would have been obvious to one having ordinary skill in the computer art at the time Applicant made the invention to adapt Levine's teachings onto the admitted prior art because Levine teaches one to analyze system performance and to focus particular sets of instructions for examining the performance bottleneck.

Office Action dated May 18, 2006, page 6.

A fundamental notion of patent law is the concept that invention lies in the new combination of old elements. Therefore, a rule that every invention could be rejected as obvious by merely locating each element of the invention in the prior art and combining the references to formulate an obviousness rejection is inconsistent with the very nature of "invention." Consequently, a combination of references made to establish a *prima facie* case of obviousness must be supported by some teaching, suggestion, or incentive contained in the prior art which would have led one of ordinary skill in the art to make the claimed invention.

The Examiner bears the burden of establishing a *prima facie* case of obviousness based on the prior art when rejecting claims under 35 U.S.C. § 103. *In re Fritch*, 972 F.2d 1260, 23 U.S.P.Q.2d 1780 (Fed. Cir. 1992). The requirements for establishing a *prima facie* case of obviousness in view of a combination of references are set forth in detail in Section 2142 of the MPEP and include the requirements that the Examiner explain in detail why the combination of the teachings is proper, that the Examiner provide a clear and convincing line of reasoning as to why an artisan would have found the claimed invention obvious in light of the teachings of the references, and that the Examiner provide a showing that it is the prior art and not the Applicant's own disclosure that teaches the combination asserted by the Examiner.

Applicants submit that the Examiner has not established a *prima facie* case of obviousness with respect to the claims. As discussed in detail above, Levine does not disclose or suggest "one or more hardware counters located within the performance monitoring unit; wherein the one or more hardware counters count the occurrence of events during processing of an interrupt of a selected type" as recited in claim 1. The admitted prior art does not supply the deficiencies in Levine as discussed in detail above, and claims 1-6, 8-14 and 16-21 are, therefore, not obvious in view of the admitted prior art and Levine,

and are allowable thereover in their present form. Applicants believe that only Applicants' disclosure teaches the combination asserted by the Examiner, and that the Examiner is using hindsight in attempting to combine the admitted prior art with Levine in an effort to achieve the present invention.

Therefore, the rejection of claims 1-6, 8-14 and 16-21 under 35 U.S.C. § 103 has been overcome.

IV. 35 U.S.C. § 103, Obviousness – Claims 7, 15, and 22

The Examiner has rejected claims 7, 15, and 22 under 35 U.S.C. § 103(a) as being unpatentable over Levine et al. (U.S. Patent No. 5,691,920) in view of previously cited "Computer System Architecture" by Morris Mano or as being unpatentable over the admitted prior art in view of Levine and Mano. These rejections are respectfully traversed.

Mono is cited as disclosing monitoring interrupts according to their priority. Mono does not, however, disclose counting events separately that occur "during the processing of the interrupt of the selected type and during processing of the second interrupt" that interrupts the interrupt of the selected type as recited in claim 7. Further, Mano does not supply the deficiencies in Levine or in Levine and admitted prior art. Claim 7 and corresponding claims 15 and 22, accordingly, are allowable in their present form, and it is respectfully requested that the Examiner so find.

Therefore, the rejection of claims 7, 15, and 22 under 35 U.S.C. § 103 has been overcome.

V. Conclusion

For all the above reasons, it is respectfully urged that claims 1-22 are allowable in their present form, and that this application is now in condition for allowance. It is, accordingly, respectfully requested that the Examiner so find and issue a Notice of Allowance in due course.

The Examiner is invited to call the undersigned at the below-listed telephone number if in the opinion of the Examiner such a telephone conference would expedite or aid the prosecution and examination of this application.

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Respectfully submitted,

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